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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,433	03/31/2004	Simon Knowles	321546US	3801

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HITT GAINES P.C.
P.O. BOX 832570
RICHARDSON, TX 75083

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
03/10/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/813,433	KNOWLES, SIMON	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

- In line 12, insert a comma after "unit".
- In line 13, replace "instructions and is" with --instructions, is--.
- In line 13, replace "instruction" with --instructions--.

Appropriate correction is required.

3. Claim 22 is objected to because of the following informalities:

- In line 13, delete the comma.
- Also, the examiner would like applicant to confirm that a plurality of instructions are decoded to detect whether a data processing instruction defines a fixed or configurable instruction, as set forth in lines 11-12 of the claim. More common would be simply decoding the data processing instruction to determine if it defines a fixed or configurable instruction. It is not clear why multiple instructions need to be decoded to make such a determination.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 1-21 are rejected under 35 U.S.C. 101 because claims 1-21, under one broad and reasonable interpretation, are directed to software per se (for instance, a system of VHDL components modeling hardware), as claims 10-21 include no explicit recitation of any hardware component, nor do they include any component which must be interpreted solely as hardware. Please amend claim 1 to explicitly recite the word "hardware" such that at least one hardware component is explicitly claimed. For instance, "hardware" may be inserted before "computer" in line 1, before "decode" in line 3,before "control" in line 4, before any of the components in line 5, etc.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, U.S. Patent No. 5,737,631, in view of Haynes et al., "Configurable Multiplier Blocks for use within an FPGA", 1998 (herein referred to as Haynes), Lodi et al., "A Flexible LUT-Based Carry Chain for FPGAs", 2003 (herein referred to as Lodi), and Madurawe, U.S. Patent No. 7,176,713.

8. Referring to claim 1, Trimberger has taught a computer processor having control and data processing capabilities comprising:

a) a decode unit for decoding instructions (Trimberger: Figure 2, item 112).

b) a dedicated control processing facility comprising a control execution path having its own control register file (Fig.2, component 103 or 140, for instance) and an execution unit (Fig.2, component 100). Note that at least these components may be combined and called a dedicated control processing facility.

c) a dedicated data processing facility (Fig.2, at least component 120), separate from said dedicated control processing facility, having its own data register file (Fig.2, at least component 130) separate from said control register file, the data processing facility comprising a controller (controllers inherently exist in processors).

d) Trimberger has not taught that the data processing facility comprises a first data execution path including fixed operators and a second data execution path including at least configurable operators, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes. However, Haynes, Lodi, and Madurawe have taught that FPGAs may be designed to include dedicated circuitry in addition to reconfigurable circuitry. Specifically, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form, among other things, absolute value and logic function circuitry. See page 133 and sections 3.3 and 4. Madurawe has taught dedicated adders and I/O circuitry in an FPGA for common operations. See column 6, lines 2-4. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes, Lodi, and Madurawe have taught programmable devices, such as FPGAs, that include fixed and configurable circuitry. Such a configuration,

which is common in a Xilinx Virtex FPGA, for instance, allows programmers to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes, Lodi, and Madurawe could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve increased speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, in order to increase speed for common operations, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array such that the data processing facility (Trimberger, Fig.2, at least component 120) comprises a first data execution path including fixed operators (for instance, a fixed adder and I/O path, as taught by Madurawe) and a second data execution path including at least configurable operators (for instance, a configurable multiplier and carry-chain path, as taught by Haynes and Lodi), both of said first and second data execution paths separate from said control execution path and each other (clearly the FPGA paths are separate from each other and from the control path), said configurable operators pre-configured into a plurality of hardwired operator classes (in the proposed combination, the FPGA of Trimberger, as modified, would include configurable operators pre-configured into hardwired multiplier and carry chain classes).

d) Trimberger has further taught that said decode unit which separates control instructions from data processing instructions and is operable to detect whether one of said data processing instructions defines a fixed data processing instruction or a configurable data processing instruction, said decode unit causing the computer processor to supply said data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable

data processing instruction is detected. See Fig.2, component 112 and column 7, lines 45-50. The examiner asserts that decoders inherently operation in the claimed fashion. They distinguish all types of instructions from each other, and produce the appropriate control signals 113 to control the appropriate circuitry to perform the desired operation.

e) Trimberger has not taught that the dedicated control processing facility also includes a branch unit (despite hinting at existence of a branch unit with disclosure of condition codes (Fig.2)) and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

f) Trimberger, as modified, has further taught that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction. See column 3, lines 31-33, and note that Trimberger would still select the connectivity of the operator classes via program instruction opcode.

9. Referring to claim 2, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of

instruction packets from memory, each packet comprising a plurality of instructions (Trimberger: column 7, lines 51-56).

10. Referring to claim 3, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction (Trimberger: column 7, lines 45-50).

11. Referring to claim 4, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the configurable operators are configurable at the level of multi-bit values (Trimberger: column 9, lines 18-19) (The opcode is a multi-bit value).

12. Referring to claim 5, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of multi-bit values comprising four or more bits (Trimberger: column 9, lines 18-19) (The opcode is at least 4 bits).

13. Referring to claim 6, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of words (Trimberger: column 9, lines 24-25) (Immediate values are optional; therefore, the whole word is configurable).

14. Referring to claim 7, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1. Trimberger has not taught that a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data

in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that a plurality of the fixed operators of the first data execution path (Fig.2, component 100) is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

15. Referring to claim 8, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1. Trimberger in view of Haynes and Lodi has not taught that a plurality of the configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger in view of Haynes and Lodi such that a plurality of the configurable operators of the second data execution path (Trimberger, Fig.2, component 120) is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

16. Referring to claim 9, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are

arranged to receive configuration information which determines the nature of the operations performed (Trimberger: column 8, lines 5-17).

17. Referring to claim 10, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from a field of an instruction defining a configurable data processing operation (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

18. Referring to claim 11, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling connectivity of the configurable operators (Trimberger: column 8, lines 35-37).

19. Referring to claim 12, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

20. Referring to claim 13, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators (Trimberger: column 8, lines 35-37).

21. Referring to claim 14, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction (Trimberger: column 8, lines 5-17; Figure 2; items 101, 102 and 123).

22. Referring to claim 15, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store (Trimberger: column 3, lines 10-27) (It is inherent that these complex functions will take at least two cycles).

23. Referring to claim 16, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators (Trimberger: column 7, lines 45-50).

24. Referring to claim 17, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop (Trimberger: column 8, lines 51-59).

25. Referring to claim 18, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for

supply to configurable operators of the second data execution path (Trimberger: column 3, lines 66-67; column 4, lines 1-10).

26. Referring to claim 19, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path (Trimberger: column 8, lines 5-17).

27. Referring to claim 20, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters (Trimberger: column 3, lines 10-27).

28. Referring to claim 21, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions (Trimberger: column 3, lines 10-27) (polynomial evaluation is used in FFT and IFFT).

29. Referring to claim 22, Trimberger has taught a method of operating a computer processor having control and data processing capabilities, said computer processor comprising:

a) a decode unit for decoding instructions (Fig.2, component 112).

b) a dedicated control processing facility comprising a control execution path having its own control register file (Fig.2, component 103 or 140, for instance) and an execution unit (Fig.2,

component 100). Note that at least these components may be combined and called a dedicated control processing facility.

c) a dedicated data processing facility (Fig.2, at least component 120), separate from said dedicated control processing facility, having its own data register file (Fig.2, at least 130) separate from said control register file, the data processing facility comprising a controller (controllers inherently exist in processors).

d) Trimberger has not taught that the data processing facility comprises a first data execution path including fixed operators and a second data execution path including at least configurable operators, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes. However, Haynes, Lodi, and Madurawe have taught that FPGAs may be designed to include dedicated circuitry in addition to reconfigurable circuitry. Specifically, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form, among other things, absolute value and logic function circuitry. See page 133 and sections 3.3 and 4. Madurawe has taught dedicated adders and I/O circuitry in an FPGA for common operations. See column 6, lines 2-4. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes, Lodi, and Madurawe have taught programmable devices, such as FPGAs, that include fixed and configurable circuitry. Such a configuration, which is common in a Xilinx Virtex FPGA, for instance, allows programmers to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes, Lodi, and Madurawe could be

implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve increased speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, in order to increase speed for common operations, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array such that the data processing facility (Trimberger, Fig.2, at least component 120) comprises a first data execution path including fixed operators (for instance, a fixed adder and I/O path, as taught by Madurawe) and a second data execution path including at least configurable operators (for instance, a configurable multiplier and carry-chain path, as taught by Haynes and Lodi), both of said first and second data execution paths separate from said control execution path and each other (clearly the FPGA paths are separate from each other and from the control path), said configurable operators pre-configured into a plurality of hardwired operator classes (in the proposed combination, the FPGA of Trimberger, as modified, would include configurable operators pre-configured into hardwired multiplier and carry chain classes).

e) Trimberger has further taught that the method comprises separating, with said decode unit, control instructions from data processing instructions. See Fig.2, component 112 and column 7, lines 45-50. The examiner asserts that the decoder inherently operates as claimed as the whole purpose of a decoder is to determine the type of instruction and generate the appropriate control signals 113 to control the appropriate circuitry to perform the desired operation. Clearly, if the instruction is meant for execution unit 100, then an instruction for that unit will be determined and signals for that unit will be supplied by the decoder.

f) Trimberger has further taught that the method comprises decoding a plurality of instructions to detect whether at least one of said data processing instructions of said plurality of instructions

defines a fixed data processing instruction or a configurable data processing instruction. See Fig.2, component 112. This is again deemed inherent. If an instruction is a fixed path instruction, then appropriate signals will be sent to the fixed FPGA circuitry. If the instruction is a configurable instruction, then appropriate signals will be sent to the configurable FPGA circuitry.

g) Trimberger has further taught that the method comprises causing the computer processor to supply said at least one data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable data processing instruction is detected; and outputting results produced by said first data execution path when a fixed data processing instruction is detected and outputting results produced by said data execution path when a configurable processing instruction is detected. This is deemed inherent. Clearly, if the FPGA is to perform a particular add, then the fixed adder will be used to execute the add and produce a result. Similarly, if an absolute value is to be performed, the configurable carry-chain will be used to produce a result.

h) Trimberger has not taught that the dedicated control processing facility also include a branch unit and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious

to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

i) Trimberger, as modified, has further taught configuring the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction. See column 3, lines 31-33, and note that Trimberger would still select the connectivity of the operator classes via program instruction opcode.

Response to Arguments

30. Applicant's arguments have been fully considered but are deemed non-persuasive in light of the new grounds of rejection/interpretation above. Specifically, in the new rejection, the examiner sets forth three separate execution paths. Also, the examiner asserts that a decoder inherently distinguishes between instructions as different control signals are produced in response to each instruction and sent to appropriate circuitry for control. Hence, the system must know when a fixed path instruction and a configurable path instruction are encountered.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183